

Application Serial No. 10/767,088  
Amendment dated February 28, 2006  
Amendment to Office Action mailed November 14, 2005

Docket No. CML01079J

**Amendment to the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application.

**Listing of Claims:**

1. (currently amended) A configurable circuit, comprising:  
a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs;  
the variable length delay line having a number of active delay elements determined by a program command; and  
a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements, the configurable processing array generating a periodic output in response to each program command.
2. (Original) The configurable circuit according to claim 1, further comprising a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements.
3. (Currently Amended) The configurable circuit according to claim 1, wherein the delay of the N delay elements is controlled by a control processor, the control processor comprising one of: data information logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a multiplexer, and multiplexer in conjunction with an ALU.
4. (Original) The configurable circuit according to claim 1, wherein the delay of the N delay elements is controlled by an output of a delay locked loop.

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5. (Original) The configurable circuit according to claim 1, wherein each of the N delay elements comprises a pair of series connected inverters.
6. (Original) The configurable circuit according to claim 1, wherein the configurable processing array further comprises an input and an output that can be configured under program control.
7. (Original) The configurable circuit according to claim 1, wherein the configurable processing array further comprises a plurality of outputs that can be configured under program control.
8. (previously presented) The configurable circuit according to claim 1, wherein the configurable processing array comprise a plurality of configurable processing units (PUs).
9. (previously presented) The configurable circuit according to claim 1, wherein the configurable processing array comprise a programmable logic device.
10. (previously presented) The configurable circuit according to claim 1, further comprising a programmable multiplexer, responsive to a program control command to selectively enable a selected group of delay elements while disabling remaining delay elements.

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11. (currently amended) A configurable circuit, comprising:  
a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs;  
the N delay elements each comprising a pair of series connected inverters;  
the variable length delay line having a number of active delay elements determined by a program command;  
a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements, the configurable processing array generating a periodic output in response to the program command;  
a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements; and  
a delay locked loop controlling the delay of the N delay elements.

12. (currently amended) The configurable circuit according to claim 11, wherein the configurable processing array further comprises an input, and wherein the configurable processor array input and an output that can be are configured under program control of a control processor including one of: data formatting logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a multiplexer, and multiplexer in conjunction with an ALU.

13. (Original) The configurable circuit according to claim 11, wherein the configurable processing array further comprises a plurality of outputs that can be configured under program control.

14. (Original) The configurable circuit according to claim 11, wherein the configurable circuits comprise a plurality of configurable processing units (PUs).

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15. (Original) The configurable circuit according to claim 11, wherein the configurable circuits comprise a programmable logic device.

16. (Original) The configurable circuit according to claim 11, further comprising a programmable multiplexer, responsive to the program control command to selectively enable a selected group of delay elements while disabling remaining delay elements.

17. (currently amended) A method of performing a circuit function, comprising:  
applying an input to a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs, the variable length delay line having a number of active delay elements determined by a program command; and  
applying the delayed outputs of the active delay elements to a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements that have been configured under program control to carry out a circuit function wherein a periodic output is generated in response to the program control.

18. (Original) The method according to claim 17, further comprising programming the variable length delay line and the configurable processing array using a control processor that configures the number of active delay elements of the variable length delay line and configures the circuit function of the array of configurable circuit elements.

19. (Original) The method according to claim 17, further comprising controlling the delay of the N delay elements to achieve a selected overall delay.

20. (currently amended) The method according to claim 17, wherein the configurable processing array further comprises an input and an output that are configured under program control, the configurable processing array comprising one of: data formatting logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a multiplexer, and a multiplexer in conjunction with an ALU.

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21. (Original) The method according to claim 17, wherein the configurable circuits comprise at least one of a plurality of configurable processing units (PUs) and a programmable logic device.

Claims 22 – 28 (Canceled)

29. (currently amended) A configurable circuit, comprising:

a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs, wherein each of the N delay elements comprises a pair of series connected inverters;

the variable length delay line having a number of active delay elements determined by a program command;

a configurable processing array comprising a plurality of configurable processing units (PUs), the configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements;

wherein the configurable processing array further comprises an input and a plurality of outputs that can be configured under program control; and

a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements and wherein the delay of the N delay elements is controlled by a control processor, wherein the configurable processing array generates a periodic output in response each program command.